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Retiming of Circuits Using Clock Management Techniques

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Abstract

Retiming is one of the most powerful sequential transformations that relocates flip-flops in a circuit without changing its functionality and that optimizes the sequential circuit which improves performance. It is the concept of improving the timing behavior of a circuit by relocating flip-flops across logic gates to achieve faster clocking speed. It decreases the iteration period without affecting functionality. A lower iteration period implies faster execution. This paper proposes different clock management techniques which were implemented in asynchronous counter to minimize the clock period. In this work net skew and maximum delay of the clock and average connection delay, maximum pin delay and connection delay on critical nets will be compared. The Xilinx ISE Design suite, Modelsim-Altera has been used for simulation and programming was done in VERILOG model.

Keywords:*clock,retiming, iteration period, speed, delay.*

1. Introduction

Retiming is a sequential optimization technique that relocates flip-flops within a circuit without altering the functionality [1]. As relocating the flip-flops balances the critical path and minimizes the states of the circuit, implementation of clock management techniques can minimize the clock period. In this paper clock period minimization with retiming has been discussed. Clock signal, which is important used for synchronization of data in sequential circuits [2]. The circuits using clock signal will become active at rising and falling edges of signal. It works with high frequency. Minimum period retiming is used to minimize the clock period [3]. It has many applications in sequential circuit design which includes clock period minimization, reducing logic synthesis and power consumption inthe circuits. It can be used to increase the rate of the clock by reducing delay on critical nets [4]. Retiming can be used to increase the clock rate of a circuit by reducing the computation time of critical path.The critical path is the path with maximum delay and is also known as longest path [10]. However, interconnect delayand clock skew are the important factors to decide the performance of the circuit.Clock skew is the difference between the minimum and maximum path delays which includes logic delays [12]. The interconnect delay is nothing but delay of the wires between thecomponents in the circuit.Existing circuit is mod-4 asynchronous counter which counts 0, 1, 2 and 3. The negative edge of the clock is used for synchronization of the asynchronous circuit.In Section 2; the theory about asynchronous counters has been described.Section 3,describes the clock management techniques, Section 4 is about simulation result and comparison of delays and Section 5 is about conclusion.References are described inSection 6.

2. Asynchronous Counters

Asynchronous counter is also known as a ripple counter. The output of one flip-flop acts as input to the other flip-flop. The clock inputs of all the flip-flops are not triggered by the incoming pulses but by the transitions occur in other flip-flops [2]. The circuit counts at falling edge of the clock i.e. the circuit is synchronized by negative edge of clock. In asynchronous counter events do not occur at the same time. The flip-flops would not change states exactly at same time because clock pulses do not connected to the clock input of the circuit [4].

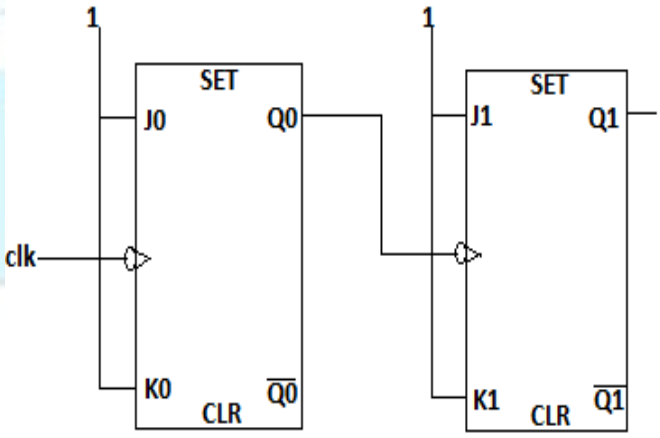

Fig.1. Mod-4 asynchronous counters [2]

Mod-4 counter is 2 bit counter which counts 0 to 3. In this work existing circuit is mod-4 counter which is implemented with pipelining at clock path and data path,

buffer insertion and register insertion at resistive path in the circuit.

3.Clock Management Techniques

Pipelining, padding and register insertion are the different techniques implemented in asynchronous counter [5]. Pipelining reduces the critical path by placing latches along path in the circuit.The minimum period possible under retiming is restricted by a critical cycle [6]. In this latches are placed in a path to minimize clock period. In pipelining, data processing elements are connected in sequence, so that the output of one block is the input to next block [11],[13].The elements of a pipeline are often executed in parallel or time sliced fashion.

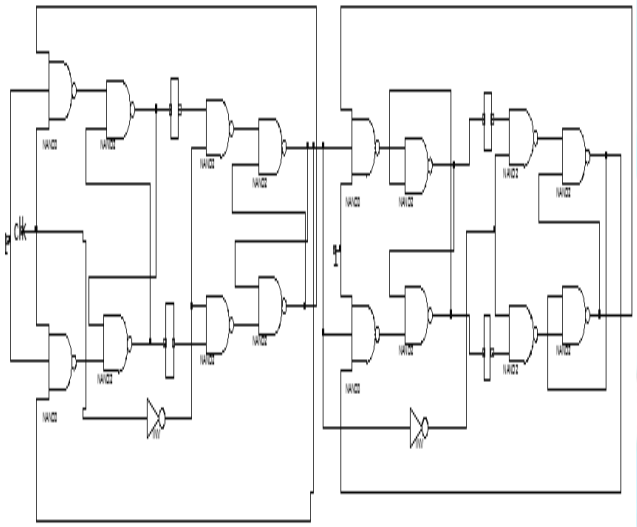

Fig.2. Pipelining in data path

Pipelining transformation leads to a reduction in the critical path i.e. longest path, which can be used to increase the clock speed by using registers along the path.The path with maximum delay is the critical path [7].In this new signals will compute simultaneously, new circuitcomputations are able to begin while previous computations are still in progress. Pipelining has been implemented at clock path and data path in the circuit [14].

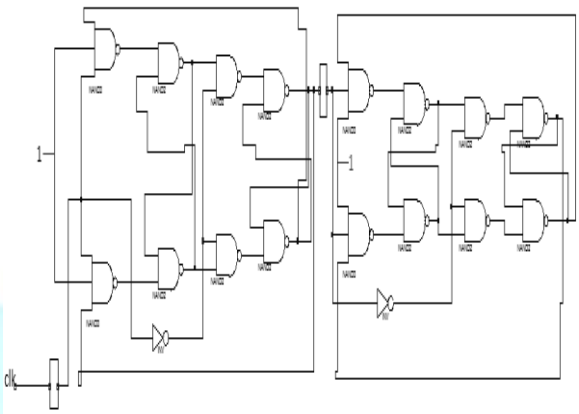

Fig.3. Pipelining in clock path

Padding is nothing but buffer insertion at longest path or critical path. Clock skew scheduling is a useful sequential optimization to improve circuit speed [8].

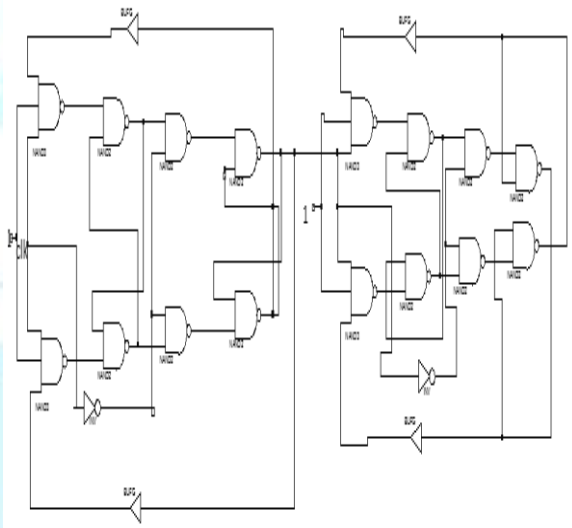

Fig.4. Padding in critical path

By properly scheduling the clock arrival times of registers, the clock period of a nonzero clock skew circuit can be shorter than the longest path delay [9]. However, due to the hold timings limitation, clock skew minimization often cannot gain the lower bound for sequential optimization [8].A hold violation means the previous data is not held long enough at the next register. Therefore, the hold

violations for achieving the lower bound of sequential timing minimization can be resolved by applying the delay insertion which is known as padding method [5].

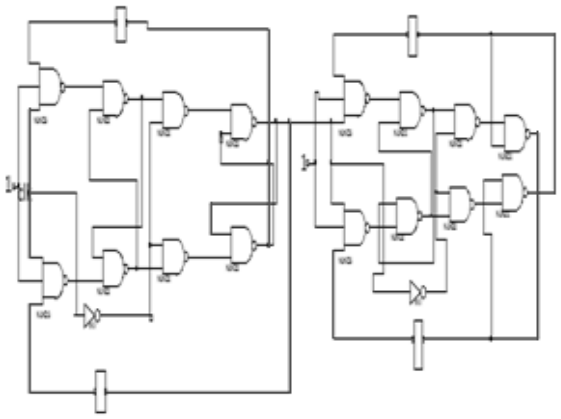

Fig.5. Register insertion at critical path

In longest path which is having more delay insertion of registers and buffers at that path will reduces clock skew [5] and wire delays and pin delays which are main causes of clock skew are reduced. Buffers will amplify the signal when it is placedat the critical paths of the circuit [2].

4. Simulation Results

These graphs represent the simulation result of register insertion at critical path, pipelining in clock path, padding at critical path, pipelining in data path. Simulation has done using Xilinx Software. In Comparison table different delays are discussed.

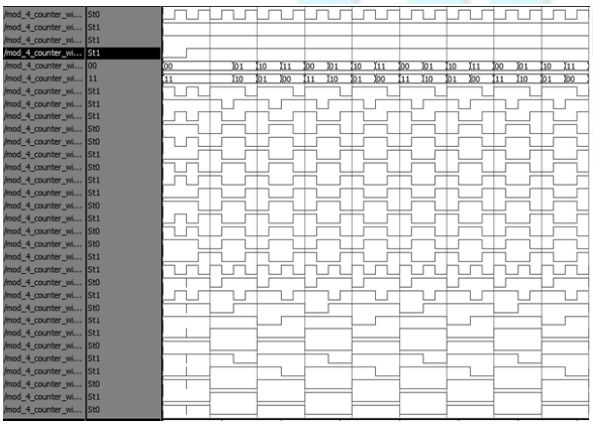

Fig.6. Pipelining in data path

Fig 6 describes the output of the circuit with implementation of pipelining in data path. Pipelining latches are placed in between master and slave section of counter circuit. When clock is negative edge triggered, if reset is '1', at enable '1' and at clear '0' circuit will be at initial state and when clear is '1' circuit starts counting.

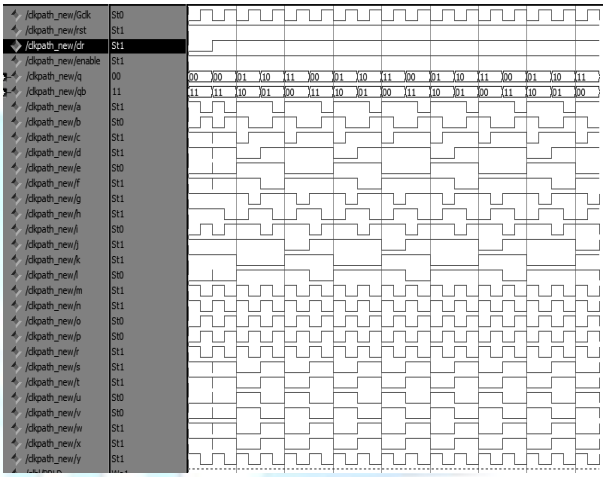

Fig.7. Pipelining in clock path

Fig 7 describes the response of the circuit with pipelining at clock inputs. When reset is '1', enable is '1' and clear is '0' counter will come to initial state and when clear is '1' circuit counts from 0, 1, 2 and 3. D-latch has been used for pipelining in clock path of asynchronous counter.

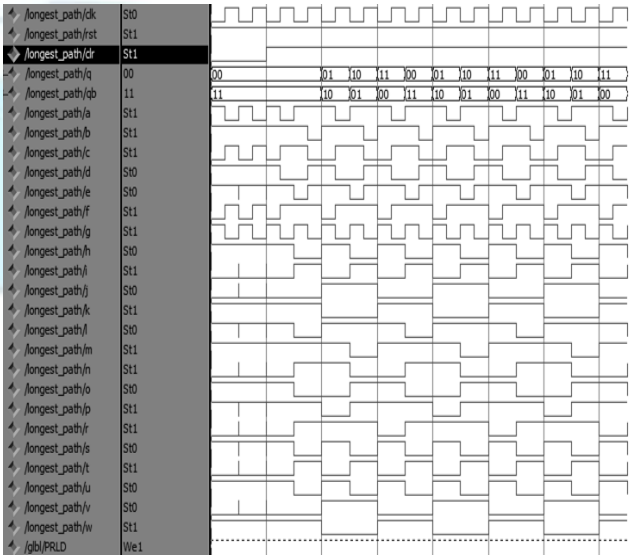

Fig.8. Padding at critical path

Fig 8 describes the output related to padding at resistive path in the circuit. Buffers are inserted at more resistive path in the asynchronous counter, when negative edge triggered clock, if reset is '1', clear is '0' circuit reaches initial state and when clear is '1' startscounting.

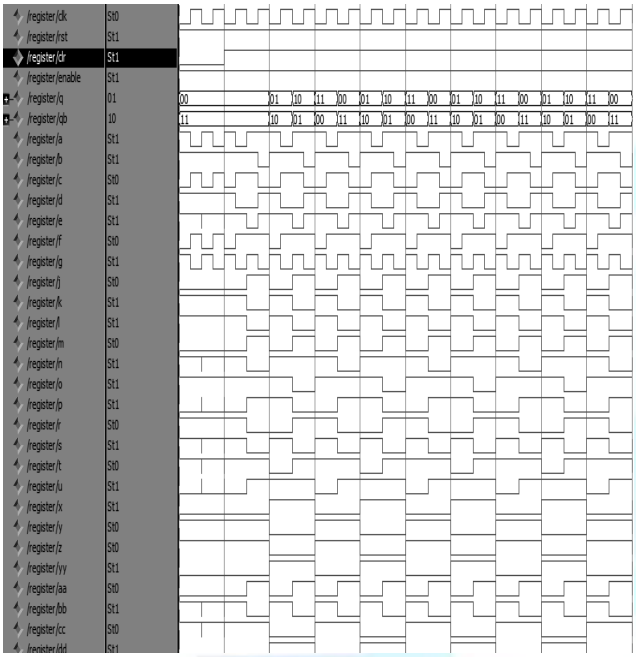

Fig.9. Register insertion at critical path

Fig 9 represents the result about the register insertion at resistive path in the circuit. Registers are inserted at more resistive path in the mod-4 asynchronous counter, when clock is negative edge triggered, if reset is '1',clear is '0' and enable is '1' then counter will come to initial state and when clear is '1' circuit starts counting from 0,1,2 and 3.

The following table describes comparison of net skew, maximum delay of clock signal of asynchronous counter implemented with different clock management techniques and also describes average connection delay of circuit, maximum pin delay and average connection delay on critical nets in the asynchronous circuit. The net skew was 0.019 ns for existing circuit and 0.004 ns for the circuit implemented pipelining in clock path. The maximum delay of clock was 0.741 ns for existing circuit and 0.046 ns for proposed circuit. The wire delay on critical nets was 1.214 ns for existing and 1.007 ns for the circuit with pipelining at clock input. These values are from clock report and delay summary report of the place and route report from Xilinx ISE simulator.

Table 1: Comparison of Delays

Parameters	***Existing counter***	***Buffer insertion***	***Registerinsertion***	***Pipelining in clock path***	***Pipelining in data path***
Net Skew (ns)	0.019	0.002	0.001	0.004	0.006
Max delay (ns)	0.741	0.046	1.199	0.046	0.072
Wire delay (ns)	0.895	0.714	0.678	0.606	0.786
Max pin delay (ns)	2.894	2.049	1.615	1.388	2.603
Wire delay on critical nets	1.214	0.959	0.911	1.007	1.426

5. Conclusion

In this paper, different clock management techniques are implemented in mod-4 asynchronous counter and observed the pin delay, wire delay, average wire delay on critical path nets and net skew and maximum delay of clock from place and route report of Xilinx simulator. After including techniques, the comparison of obtained results show that the maximum delay of clock with register insertion technique and wire delay on critical paths with pipelining in data path narrowly increased, but the other delays are reduced when compared to existing counter with the techniques applied. So, the proposed counter with clock management techniques is better in minimizing the clock period compared with existing counter circuit.

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